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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,274	LEHONGRE, DENIS	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/25/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 09/25/2008.

2. Claims 1-59 are pending in this application. Claims 1-2, 7-8, 15-23, 31, 37 and 54 are independent claims. In Amendment, claim 59 is added. This Office Action is made non-final after a RCE filed 09/25/2008.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert de Tremiolles et al. (U.S. 2001/0013048) in view of Reto Zimmermann ("Computer Arithmetic: Principles, Architectures, and VLSI Design").

Re claim 1, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to process digital data belonging to a set of 2.sup.n codes in which a relation of order is established and in which each of data has a rank R between 0 and 2.sup.n-1, device (e.g. abstract and Figure 4) comprising: a conversion circuit for said digital data to be processed and adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by generate a transform that is a binary number having 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1T[2.sup.n-1]T[2.sup.n-2] . . .

T[x] . . . T[2]T[1] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and circuits to receive a result of the conversion circuit and to carry out a digital processing of result (e.g. other steps as seen in paragraphs [0015-0017]), wherein the conversion circuit is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 2, it has similar limitations cited in claim 1 wherein x = 0 and start at T[0] (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 2 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 3, Imbert de Tremiolles et al. further disclose in Figures 2-6 characterized in that digital processing includes a Boolean OR carried out in bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of transform, in order to read out a maximum value of a set of digital values (e.g. paragraph [0014]).

Re claim 4, Imbert de Tremiolles et al. further disclose in Figures 2-6 the read out of maximum value is followed by a comparison with another value (e.g. abstract and paragraph [0011]).

Re claim 5, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean AND, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of transform, in order to read out a minimum value of a set of digital values (e.g. paragraphs [0011-0017]).

Re claim 6, it has similar limitations cited in claim 4. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 7, it has similar limitations cited in claim 1 wherein x = 1 and start at T[1]; T(x) =1 and T(x) = 0 respectively (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, it has similar limitations cited in claim 1 wherein x = 0 and start at T[0]; T(x) 1 and T(x) = 0 respectively (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, it has similar limitations cited in claim 5. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 10, it has similar limitations cited in claim 6. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 11, it has similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it has similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, Imbert de Tremiolles et al. does not disclose in Figures 2-6 the original code of the digital data to process be processed further includes an unsigned type, Gray, Johnson, and includes a mantissa and an exponent. However, Reto Zimmermann discloses in the articles the original code of the digital data to process be processed further includes an unsigned type, Gray, Johnson, and includes a mantissa and an exponent (e.g. section 3 in pages 10-19 and 57-59).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the original code of the digital data to process be processed further includes an unsigned type, Gray, Johnson, and includes a mantissa and an exponent as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 14, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in

sequence various parts of each data (e.g. by feedback loop for all the sub-group in Figure 4).

Re claim 15, it has similar limitations cited in claim 3. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 16, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data as a code having 2.sup.n binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]) wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 17, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1, device (e.g. abstract and Figure 4) comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]) ; and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said

transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 18, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4

and paragraph [0014]) ; and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 19, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs

[0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 20, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 21, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 22, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to read out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to represent each one of digital data under a form of a code made up of 2.sup.n binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]), wherein the circuit to reduce processing time is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform into

T[x] to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 23, Imbert de Tremiolles et al. disclose in Figures 2-6 an apparatus (e.g. abstract and Figure 4), comprising: a conversion circuit to receive digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. Figure 4 and paragraphs [0012-0014]), the conversion circuit being capable to adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by being adapted to transform the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank; and a processing circuit coupled to the conversion circuit to receive the digital data that has been transformed to the binary number and to

generate a result therefrom (e.g. paragraphs [0011-0017]), wherein the conversion circuit is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 24, Imbert de Tremiolles et al. further disclose in Figures 2-6 the conversion circuit includes a plurality of conversion units, each being capable to transform their respective digital data from the set into a binary number (e.g. Figures 2-4).

Re claim 25, Imbert de Tremiolles et al. further disclose in Figures 2-6 the processing circuit (e.g. Figure 4 and abstract) includes: a first unit coupled to the conversion circuit to apply a logical operation on binary numbers received from the

conversion circuit to generate at least one output therefrom (e.g. Figures 2); and a second unit coupled to the first unit to perform a reverse transform on the at least one output from the first unit to generate the result (e.g. paragraphs [0007-0027]).

Re claim 26, Imbert de Tremiolles et al. further disclose in Figures 2-6 the logical operation comprises a logical OR operation carried out in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 27, Imbert de Tremiolles et al. further disclose in Figures 2-6 the logical operation comprises a logical AND operation carried out in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 28, Imbert de Tremiolles et al. further disclose in Figures 2-6 the result includes a minimum value of the set of digital data (e.g. abstract).

Re claim 29, Imbert de Tremiolles et al. further disclose in Figures 2-6 the result includes a maximum value of the set of digital data (e.g. abstract).

Re claim 30, Imbert de Tremiolles et al. further disclose in Figures 2-6 at least another circuit coupled to the processing circuit to compare the result with another value (e.g. Figures 2).

Re claim 31, Imbert de Tremiolles et al. further disclose in Figures 2-6 a method (e.g. abstract and Figure 4), comprising: receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. step A in Figure 4); adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by transforming each of the received digital data into a binary number having binary elements whose values are based

at least in part on a value of the rank (e.g. steps B - step D in Figure 4); and processing the digital data that has been transformed into the binary numbers to generate a result therefrom (e.g. output of Figure 4), wherein the electronic device is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 32, Imbert de Tremiolles et al. further disclose in Figures 2-6 processing the digital data that has been transformed into the binary numbers (e.g. abstract and Figure 4) includes: applying a logical operation on the binary numbers to generate at least one output therefrom (e.g. paragraphs [0011-0017]); and performing a reverse transform on the at least one output to generate the result (e.g. paragraphs [0007-0027]).

Re claim 33, Imbert de Tremiolles et al. further disclose in Figures 2-6 applying the logical operation includes applying a logical OR operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 34, Imbert de Tremiolles et al. further disclose in Figures 2-6 applying the logical operation includes applying a logical AND operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 35, Imbert de Tremiolles et al. further disclose in Figures 2-6 generating the result includes at least one of generating a maximum and a minimum value of the set of digital data (e.g. paragraphs [0011-0012]).

Re claim 36, Imbert de Tremiolles et al. further disclose in Figures 2-6 comparing the generated result with another value (e.g. Figures 2).

Re claim 37, Imbert de Tremiolles et al. disclose in Figures 2-6 an apparatus (e.g. Figure 4 and abstract), comprising: a means for receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. Figure 4 and paragraphs [0011-0013]); a means for adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by transforming each of the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank (e.g. encoder in paragraph [0014]); and a means for processing the digital data that has been transformed into the binary numbers to generate a result therefrom (e.g. other steps in Figure 4), wherein the means for reducing processing is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform to be performed within the

semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the means for reducing processing time produces higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 38, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for processing the digital data that has been transformed into the binary numbers includes: a means for applying a logical operation on the binary numbers to generate at least one output therefrom; and a means for performing a reverse transform on the at least one output to generate the result (e.g. output of Figure 4).

Re claim 39, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for applying the logical operation includes at least one of a means for applying a logical OR operation and a logical AND operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 40, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for processing the digital data to generate the result includes at least one of a means for generating a maximum and a minimum value of the set of digital data (e.g. abstract and Figure 4).

Re claim 41, Imbert de Tremiolles et al. further disclose in Figures 2-6 a means for comparing the generated result with another value (e.g. Figures 2).

Re claim 42, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean OR, carried out in bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the maximum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 43, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean AND, carried out in a bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the minimum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 44, Imbert de Tremiolles et al. further disclose in Figures 2-6 a digital processing is a Boolean AND, carried out in a bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the maximum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 45, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean OR, carried out in a bit-serial way on the bits of same index of

the transformed data and followed by a conversion which is the reverse of transform, in order to read out the minimum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 46, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 47, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 48, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 49, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 50, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 51, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 52, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 53, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 54, Imbert de Tremiolles et al. disclose in Figures 2-6 a device to process digital data belonging to a se of 2n codes in which a relation of order is established and in which each of data has a rank R comprised between 0 and 2n-1 (e.g. abstract and Figure 4), the device comprising: a conversion circuit for each digital data to be processed and adapted to reduce processing time of a high volume of the data by computer (e.g. paragraphs [0002 and 0007-0009]), by generate of a transform that is a binary number composed of 2n-1 binary elements T[x] with x=a to 2n-1 with a and b being equal to 0 or 1, wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and circuits to receive a result of the conversions and to carry out a digital processing of the circuit (e.g. paragraphs [0011-0017]), wherein the conversion circuit is integrated in a semiconductor circuit (e.g. paragraph [0002]) so as to enable said transform to be performed within the semiconductor circuit to increase data processing speed (e.g. abstract and paragraph [0007]), and wherein the conversion circuit is adapted to produce higher processing timesaving as a number of the digital data to be processed gets larger (e.g. abstract by the last four lines).

Imbert de Tremiolles et al. does not expressively define an original code of the digital data to be processed includes a signed type. However, Reto Zimmermann discloses in the article the digital data to be processed includes a signed type (e.g. section 3 in pages 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an original code of the digital data to be processed includes a signed type as seen in Reto Zimmermann's invention into Imbert de Tremiolles et al.'s invention because it would enable to enhance the system performance with multiple data types.

Re claim 55, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (1,1) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 56, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (0,0) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 57, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (0,1) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 58, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (1,0) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 59, the conversion circuit is adapted to simultaneously carry out each of the transform of the data (e.g. paragraph [0007]).

Response to Arguments

5. Applicant's arguments with respect to claims 1-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

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